Lateral variations in threshold voltage of an $Al_xGa_{1-x}N$/GaN heterostructure field-effect transistor measured by scanning capacitance spectroscopy

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Local dC/dV spectroscopy performed in a scanning capacitance microscope (SCM) was used to map, quantitatively and with high spatial resolution ($\sim$50 nm), lateral variations in the threshold voltage of an $Al_xGa_{1-x}N$/GaN heterostructure field-effect transistor epitaxial layer structure. Scanning capacitance and the associated threshold voltage images show small round features less than 150 nm in diameter with a corresponding shift in threshold voltage of about 1.5–2 V, and larger features several microns in size with a corresponding shift in threshold voltage of approximately 1 V. The small features in the SCM and threshold voltage images are consistent with the presence of charged threading dislocations, while the variations in threshold voltage over large areas could be a result of thickness and/or composition variations in the $Al_xGa_{1-x}N$ layer. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1335840]

$Al_xGa_{1-x}N$/GaN heterostructure field effect transistors (HFETs) have attracted intense research interest due to their importance for microwave and high-temperature/high-power electronic applications[1–4] However, high threading dislocation densities ($\sim 10^8$–10^{10} cm^{-2}), are typically present and can lead to increased carrier scattering[5] and high concentrations of acceptor-like trap levels.[6] In addition, it has been observed that the HFET threshold voltage (V_T) can shift by up to 1.5 V near a dislocation;[7] the presence of thickness and composition variations in the $Al_xGa_{1-x}N$ layer can result in further variations in V_T.[8,9] Thus far, however, only limited quantitative experimental information is available to directly correlate shifts in threshold voltage with threading dislocations, thickness and composition variations, and other defects.

In this letter, we report on the application of spatially resolved scanning capacitance spectroscopy to quantify local threshold voltages and to map threshold voltage variations for an $Al_xGa_{1-x}N$/GaN HFET; the observed shifts in V_T and their spatial distribution are consistent with the presence of charged threading dislocations and with localized thickness and/or composition variations in the $Al_xGa_{1-x}N$ layer. All measurements were performed with grounded, p^+ Si probe tips in a Digital Instruments 3100 scanning capacitance microscope (SCM) under ambient conditions with bias applied to ohmic contacts on the sample. The sample used in these studies consisted of a 23 nm undoped $Al_{0.26}Ga_{0.74}N$/1.2 μm undoped GaN/0.1 μm AlN heterostructure grown on 4H–SiC(0001) by metalorganic chemical vapor deposition. Ohmic contacts were made to the sample by evaporation of 33 nm Ti/77 nm Al and subsequent annealing at 750 °C for 1.5 min. Due to polarization effects, a two-dimensional electron gas (2DEG) is created at the $Al_xGa_{1-x}N$/GaN interface, even in the absence of intentional doping.[10–12]

Figure 1 shows scanning capacitance images and the corresponding contact-mode topography images. The scanning capacitance data were acquired with a dc bias of 5 V applied to the sample for (a), and 7 V for (b), while the ac bias was fixed at 2 V at a frequency of 100 kHz. Small round features with radii of 50–70 nm are observed in the top scanning capacitance image, while the large-area scan shows features typically several microns in size, which are similar, but do not directly correlate, to the structure observed in the topography image.

To obtain a high-resolution threshold voltage map, we

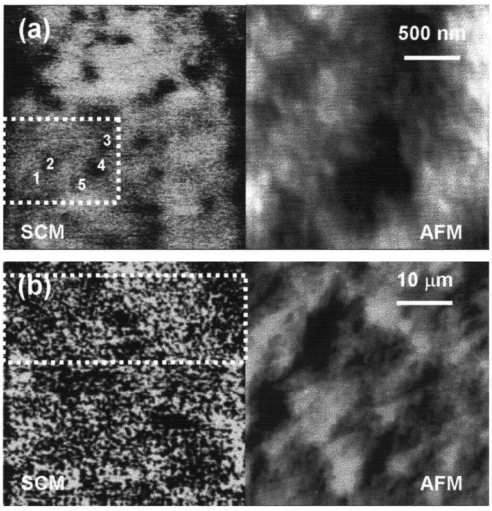

FIG. 1. Scanning capacitance (left-hand side) and atomic force (right-hand side) microscopy images of (a) a 2 μm$\times$2 μm, and (b) a 40 μm$\times$40 μm scan area. Locations where data for Fig. 2 were taken are marked by ''1'' and ''2.'' The dashed boxes indicate the areas in which threshold voltage maps were taken (see Fig. 3).

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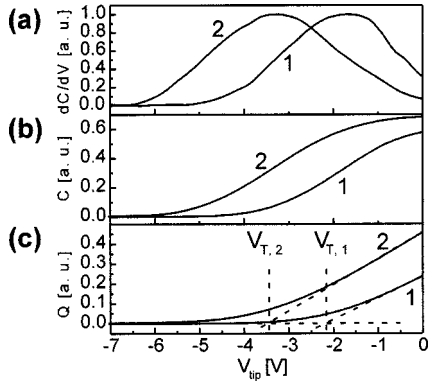

FIG. 2. (a) Plots of local dC/dV vs tip bias V_{tip}, taken at the locations indicated in Figs. 1(a) and 3(a) by ''1'' and ''2.'' (b) Capacitance–voltage characteristics, obtained by integration of the dC/dV data in (a). (c) The charge Q in the two-dimensional channel of the $Al_xGa_{1-x}N/GaN$ HFET, obtained by integration of the $C-V$ curves in (b). The threshold voltage is given by the intercept of two linear fits to the linear regions.

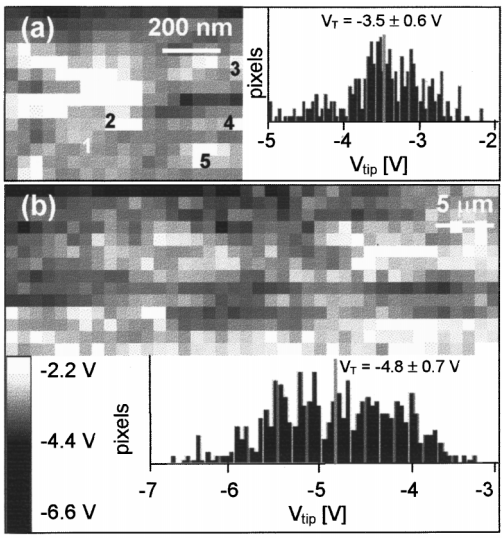

FIG. 3. Threshold voltage maps and corresponding histograms of the areas indicated by dashed boxes in Fig. 1. The scan sizes are (a) 950 nm $\times$700 nm and (b) 40 μm$\times$15 μm. The contrast scale for both images is shown on the lower left-hand side corner. Large variations in threshold voltage are clearly visible in both maps. Features that correspond to those observed in the SCM image in Fig. 1(a) are marked by ''1''–''5.''

reduced the scan area to 1 nm$\times$1 nm and measured the dC/dV signal from the SCM as a function of a dc bias V_{sample}. This bias was ramped from 0 to 8 V with a frequency of 5 Hz and added to the SCM ac bias. To reduce noise, we averaged multiple (typically 50–400) dC/dV vs V curves. We then moved the tip in steps of 50 nm and repeated the procedure. For low-resolution threshold voltage maps of larger scan areas, such as the 40 μm$\times$40 μm area as shown in Fig. 1, we scanned the tip at each point over an area of 500 nm$\times$500 nm, thus effectively averaging the dC/dV vs V curve over this area, and used a step size of 1 μm.

The dC/dV vs V data were processed by subtracting a linear background that arises from uncompensated stray capacitances, and then normalizing to a peak amplitude of unity. Figure 2(a) shows the dC/dV data plotted in the usual representation, i.e., versus tip bias $V_{\text{tip}}=-V_{\text{sample}}$ for two different points in the smaller scan: one on top of a round feature (denoted by ''1'' in the figures) and an area with little SCM contrast (denoted by ''2''). An integration of these data yields the capacitance–voltage characteristics shown in Fig. 2(b), and a second integration yields the charge within the 2DEG versus voltage. The threshold voltage is then obtained by linear extrapolation, as shown in Fig. 2(c).

Figure 3 shows maps of the threshold voltage within the dashed areas indicated in Fig. 1. Both small ($\sim$100–150 nm) and larger ($\sim$3–7 μm) features are observed at length scales consistent with those observed in the corresponding SCM scans. A direct correlation between the threshold voltage maps and SCM images is complicated by thermal drift of the piezo and delays in the piezo response, which can result in a slightly shifted and stretched threshold voltage map as compared to a SCM image of the same area. To highlight the correlation between the SCM images and the threshold voltage maps, five corresponding locations are marked in Figs. 1 and 3.

The statistical distributions of the threshold voltages, shown in Fig. 3, are characterized by an average value of -3.5 V and a standard deviation of 0.6 V for (a), and an average value of -4.8 V with standard deviation of 0.7 V for (b). The observed difference in the average threshold voltages for the small and large area scans is a result of the large scale variations in V_T. The large distributions in threshold voltage observed at these length scales have important implications for the reproducibility of device performance, i.e., depending on the degree and spatial distribution of localized variations in V_T, a set of devices might show a large distribution in actual transistor threshold voltage.

The small round features in the smaller scan are consistent with the presence of charged threading dislocations at a density of about 10^9 cm^{-2} in the sample. Several groups have reported that threading dislocations in III–V nitride heterostructures can produce acceptor-like trap states[6] which become negatively charged.[13,14] This charge can result in depletion of the 2DEG at the $Al_xGa_{1-x}N/GaN$ interface,[9] causing a shift in threshold voltage near the threading dislocations which would be observed in the scanning capacitance data and the V_T map.

We can estimate the effect of a charged threading dislocation on the SCM contrast feature and on the local shift in threshold voltage. Assuming a tip with a radius of curvature of 15 nm, we would estimate an actual feature radius of 35–60 nm for an observed feature radius of 50–75 nm due solely to the convolution of the actual feature with the tip shape. In addition, the observed feature radius is increased by a depletion region of about 30 nm formed by the tip in the $Al_xGa_{1-x}N$ layer. This results in a final actual feature radius of about 30 nm or smaller.

The potential due to a charged line, with screening by ionized impurities and free electrons, is given by[15]

$$U(r)=\frac{1}{4\pi\varepsilon\varepsilon_0}2q\gamma K_0\left(\frac{r}{\lambda_D}\right), \tag{1}$$

where $\lambda_D\sqrt{(kT\varepsilon\varepsilon_0)/(q^2N_d)}$ is the Debye length, ε is the relative dielectric constant, ε_0 the vacuum permittivity, q the electron charge, γ the line charge density, K_0 the modified Bessel function of the second kind of zeroth order, r the distance from the line, k the Boltzmann constant, T the tem-

perature, and N_d the background dopant density. We can use Eq. (1) to describe the potential due to a charged threading dislocation by setting $\gamma = f/c$, where f is the fraction of filled traps (ranging from 0 to 1) and c the [0001] lattice constant of $Al_xGa_{1-x}N$. Assuming a dislocation density of $10^9\,cm^{-2}$ and a background dopant density of $10^{18}\,cm^{-3}$ within the $Al_xGa_{1-x}N$ layer, one obtains[16] $f \approx 0.5$ and a Debye length of ~3.5 nm at 300 K. The effect of the potential $U(r)$ ceases to be significant when $U(r) \lesssim kT$, i.e., when $r \gtrsim 3.25\,\lambda_D$. We thus obtain an estimated feature radius of about 11 nm, which is well within the above mentioned range of 30 nm or smaller.

In the vicinity of these features, the maximum threshold voltage shift ΔV_T from the average value is about 1.5–2 V, which is consistent with previous measurements by Hansen *et al.*[7] Using the expression $Q = -C\Delta V_T$, where C is the capacitance per unit area of the $Al_xGa_{1-x}N$ barrier layer, we estimate the measured ΔV_T to correspond to a charge Q of about -3.4 to $-4.6\times10^{12}\,e/cm^2$. This value is approximately equal to the amount of charge expected to be contained, within the $Al_xGa_{1-x}N$ barrier layer and an area equal to the tip size, on a threading dislocation with linear charge density of about $-10^7\,e/cm \approx 0.5\,e/c$.

The larger features observed in Fig. 3(b) exhibit threshold voltage shifts as large as ± 1 V or more relative to the average threshold voltage value of -4.8 V. The features observed in Fig. 1(b) are comparable in size to those observed in the topography, suggesting that thickness variations in the $Al_xGa_{1-x}N$ layer might play a substantial role in the measured V_T variations, as postulated on the basis of previously reported SCM studies.[8,9] Using a theoretical expression for the sheet carrier concentration n_s in the 2DEG,[17] ΔV_T for an $Al_xGa_{1-x}N$ layer with average thickness d due to a change in thickness $\Delta d \ll 2d$ is found to be given by

$$\Delta V_T \approx \frac{\sigma_{pol} + qN_d d}{\varepsilon_0 \varepsilon}\Delta d, \tag{2}$$

where σ_{pol} is the polarization sheet charge density at the heterojunction interface and N_d the dopant concentration in the $Al_xGa_{1-x}N$ layer. For an Al concentration of 26% and $d = 23$ nm, we obtain $\sigma_{pol} \approx 1.25\times10^{13}\,e/cm^2$,[18] which results in a threshold voltage shift of about 0.25 V for a thickness change of about 1 nm.

Using a similar approach, we can also calculate that a composition variation Δx in the $Al_xGa_{1-x}N$ layer would lead to a shift in threshold voltage ΔV_T given by

$$\Delta V_T = \frac{d}{\varepsilon_0 \varepsilon}\Delta\sigma_{pol} \approx 25\,\Delta x\ \text{V}. \tag{3}$$

Thus, $\Delta x \approx 0.01$ would yield ΔV_T comparable to that of a 1 nm thickness variation. The observed larger variations in ΔV_T of more than 1 V might therefore be the consequence of a combination of thickness and composition variations in the $Al_xGa_{1-x}N$ layer.

In conclusion, we have used local dC/dV spectroscopy performed in a scanning capacitance microscope to quantify and map the threshold voltage distribution in an $Al_xGa_{1-x}N$/GaN HFET structure. We observed small round features which showed a threshold voltage shift of about 1.5–2 V compared to the average threshold voltage, and larger features several microns in size with corresponding threshold voltage shifts of up to 1 V or more. The small features exhibit approximate charge densities consistent with the presence of charged threading dislocations that cause localized reduction or depletion of carriers from the 2DEG. The estimated density of these features is $\sim 10^9\,cm^{-2}$. The larger features are postulated to arise from a combination of thickness and composition variations in the $Al_xGa_{1-x}N$ layer.

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[1] O. Aktas, Z. F. Fan, A. Botchkarev, S. N. Mohammad, M. Roth, T. Jenkins, L. Kehias, and H. Morkoc, IEEE Electron Device Lett. **18**, 293 (1997).
[2] M. A. Khan, Q. Chen, M. S. Shur, B. T. Dermott, J. A. Higgins, J. Burm, W. J. Schaff, and L. F. Eastman, Solid-State Electron. **41**, 1555 (1997).
[3] G. J. Sullivan, M. Y. Chen, J. A. Higgins, J. W. Yang, Q. Chen, R. L. Pierson, and B. T. McDermott, IEEE Electron Device Lett. **19**, 198 (1998).
[4] Y. F. Wu, B. P. Keller, S. Keller, J. J. Xu, B. J. Thibeault, S. P. Denbaars, and U. K. Mishra, Trans. Electron. **E82C**, 1895 (1999).
[5] H. M. Ng, D. Doppalapudi, T. D. Moustakas, N. G. Weimann, and L. F. Eastman, Appl. Phys. Lett. **73**, 821 (1998).
[6] F. A. Ponce, D. P. Bour, W. Gwötz, and P. J. Wright, Appl. Phys. Lett. **68**, 57 (1996).
[7] P. J. Hansen, Y. E. Strausser, A. N. Erickson, E. J. Tarsa, P. Kozodoy, E. G. Brazel, J. P. Ibbetson, U. Mishra, V. Narayanamurti, S. P. DenBaars, and J. S. Speck, Appl. Phys. Lett. **72**, 2247 (1998).
[8] K. V. Smith, E. T. Yu, J. M. Redwing, and K. S. Boutros, Appl. Phys. Lett. **75**, 2250 (1999).
[9] K. V. Smith, E. T. Yu, J. M. Redwing, and K. S. Boutros, J. Electron. Mater. **29**, 274 (2000).
[10] A. Bykhovski, B. Gelmont, and M. Shur, J. Appl. Phys. **74**, 6734 (1993).
[11] P. M. Asbeck, E. T. Yu, S. S. Lau, G. J. Sullivan, J. Van Hove, and J. M. Redwing, Electron. Lett. **33**, 1230 (1997).
[12] E. T. Yu, G. J. Sullivan, P. M. Asbeck, C. D. Wang, D. Qiao, and S. S. Lau, Appl. Phys. Lett. **71**, 2794 (1997).
[13] K. Leung, A. F. Wright, and E. B. Stechel, Appl. Phys. Lett. **74**, 2495 (1999).
[14] M. Haugk, J. Elsner, Th. Frauenheim, T. E. M. Staab, C. D. Latham, R. Jones, H. S. Leipner, T. Heine, G. Seifert, and M. Sternberg, Phys. Status Solidi B **217**, 473 (2000).
[15] B. Pördör, Phys. Status Solidi B **16**, K167 (1966).
[16] N. G. Weinmann, L. F. Eastman, D. Doppalapudi, H. M. Ng, and T. D. Moustakas, J. Appl. Phys. **83**, 3656 (1998).
[17] E. T. Yu, P. M. Asbeck, S. S. Lau, X. Z. Dang, and G. J. Sullivan, J. Vac. Sci. Technol. B **17**, 1742 (1999).
[18] E. T. Yu, *III-V Nitride Semiconductors: Applications and Devices*, edited by E. T. Yu and O. Manasreh (Gordon and Breach, London, 2000).